Hardware Implementation of Address Register Circuit on VLSI Based FPGA Device

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***Abstract* - In this study, we construct an (AR) address register that is responsive to voltage increases. We investigated the power dissipation of an address register using the Xilinx 14.1 ISE tool, and the address register code is written in the Verilog hardware description language. In this research, we employed two FPGAs, one Virtex 4 and one Virtex 5, to investigate the power consumption of AR. We measured the difference in on-chip power required by AR by increasing the voltage from 1.0 V to 2.0 V. We discovered that lowering the voltage reduces power usage. Power consumption is greater for both FPGAs at 2.0 V. Therefore, to initiate the idea of Green Communication (GC) AR should be best suited with Virtex 4 FPGA.**

Keywords: FPGA, Address Register, Power, Voltage, and Green Communication.

I. INTRODUCTION

The globe is currently confronted with a massive dilemma in the form of an energy crisis. People's demand for natural resources, i.e., non-renewable resources, is fast growing. Overconsumption, overcrowding, and bad infrastructure are the three primary drivers of this energy problem [1]. To guarantee that the planet's natural resources are not wasted, the whole world is moving towards utilizing devices which consumes low power. The devices which consume low power comes under the category of green communication [2]. Green Communication (GC) is the practice of energy resource in such a way that the present need is also fulfilled and future resources also be saved. To achieve the concept of HC in electronics world we need devices which consumes low energy [3]. For consuming low energy Field Programmable Gate Array (FPGA) devices are best suited. FPGA is a electronic devices which is made up of semiconductor materials [4]. These devices can be reprogrammed after their manufacturing. The major components of FPGA devices are shown in fig. 1.

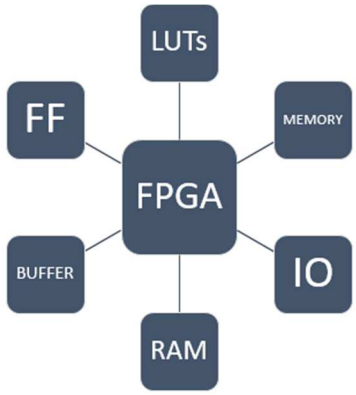

Figure 1 Major Components of FPGA Devices

In this work we are developing an AR that will demand low power in the communication system. Because our AR will require less power, hence there will be less use of power and consequently less use of the planet's natural resources which generates electricity. AR is a memory device which either stores memory or either execute data instruction. AR is also known as Memory Address Register (MAR). The working of AR is shown in fig. 2.

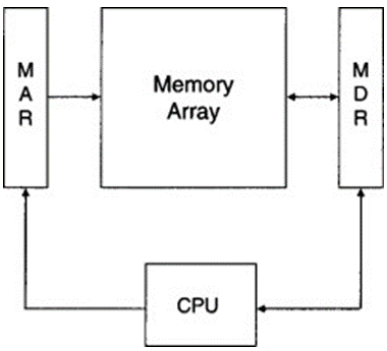

Figure 2. Working of AR

II. LITERATURE WORK

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In [5] with the help of FPGA authors have designed the control unit for enhancing the concept of GC. In [6] authors have designed the AR on various families. The FPGA used here are Viretx 6 and Spartan 6. In [7] researchers have implemented low power thermally aware control unit on FPGA devices. In [8] researches have designed a Unicode reader on FPGA device which consumes low amount of power. The power consumption techniques used here is frequency scaling. To promote GC authors have designed the instruction register by using FPGA devices [9]. In [10] LFSR circuit has been implemented by authors on FPGA to promote GC. In [11] researchers have user various FPGA to design a low power UART. In [12] authors have tested the effect of power consumption of UART on distinguished FPGA devices. With the help of impedance matching with IO standards like HSUL and HSTL authors have designed control unit for GC. In [13] by varying the capacitance of output load authors have designed a low power UART on FPGA. In [14] energy efficient transceiver has been implemented by authors for GC. From the literature work it is observed that very few work has been done to promote GC with AR. Therefore, this work highlights about the implementation of a low power AR is on FPGA device. This low power device is one of the key factors which helps in promoting the concepts of GC.

III. Experimental Setup

To design the AR in this work two FPGA devices are used such as Virtex 4 and Virtex 5 FPGA. The code of the AR for implementing the AR on FPGA is described in Verilog [15]. For analyzing the power utilization X Power Analyzer is used of Xilinx ISE tool. The technology schematic and the RTL of the AR observed on Xilinx ISE is shown in fig 3 and 4 respectively. The power consumption of the AR is tested for five different values of voltages from 1 V to 2 V for both Virtex 4 and Virtex 5 FPGA devices [16]. The five different values of voltages are such as 1.0 V, 1.25 V, 1.50 V, 1.75 V, 2.0 V.

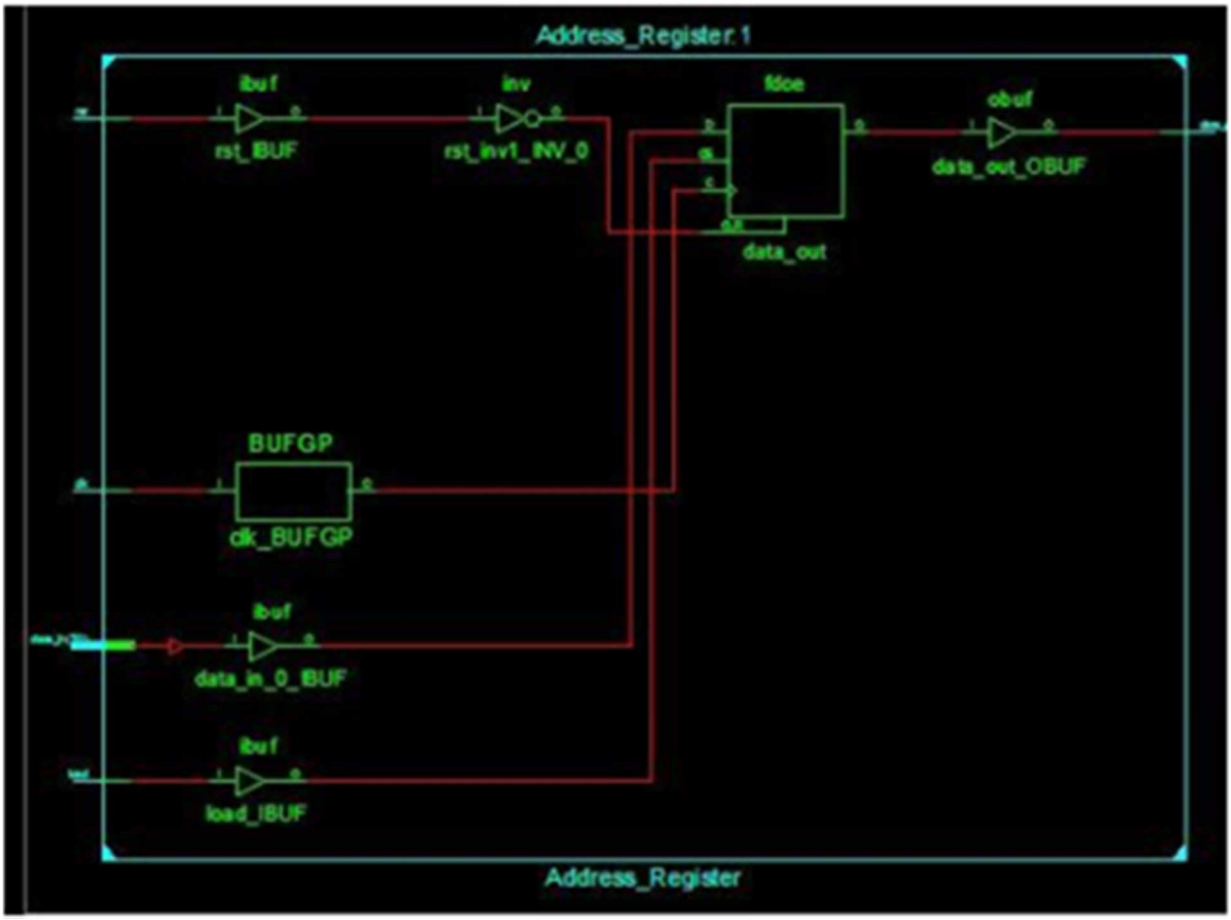

Figure 3 Technology schematic of AR observed on FPGA.

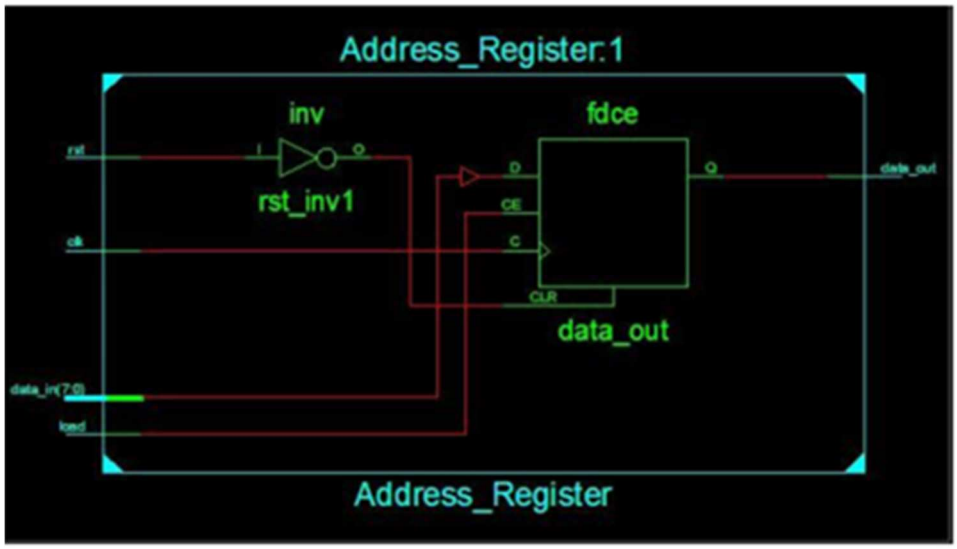

Figure 4 RTL of AR observed on FPGA

IV. Results

This section will discuss the power utilization of AR on Virtex 4 and Virtex 4 FPGA devices for five different values of voltage.

A. Power Consumption for Virtex 4 Device

The power consumption of AR on Virtex 4 FPGA increases as the value of voltage increase. For 1.0 V it is 1.2 W, for 1.25 V power consumption is 1.23 W, for 1.50 V it is 3.3 W, for 1.75 V it is 5.95 W, and for 2.0 V power consumption it is 6.3 W. The power utilization of AR for Virtex 4 device is shown in table 1 and described in fig 5.

TABLE I. Power Utilization Of Ar On Virtex Fpga

Voltage (V)	Power (W)
1.0	1.2
1.25	1.23
1.50	3.3
1.75	5.95
2.0	6.3

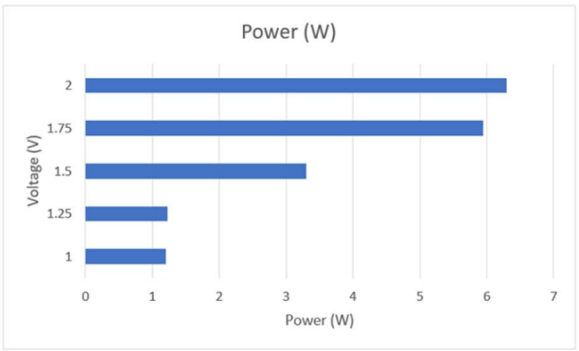

Figure 5. Power utilization of AR on Virtex 4 device

B. Power Utilization for Virtex 5 Device

The power consumption of AR on Virtex 5 FPGA increases as the value of voltage increase. For 1.0 V it is 1.26 W, for 1.25 V power consumption is 1.46 W, for 1.50 V it is 3.39 W, for 1.75 V it is 6.02 W, and for 2.0 V power consumption it is 6.48 W. The power utilization of AR for Virtex 5 device is revealed in table 2 and described in fig 6.

TABLE II. Power Utilization Of Ar On Virtex 5 Fpga

Voltage (V)	Power (W)
1.0	1.26
1.25	1.46
1.50	3.39
1.75	6.02
2.0	6.48

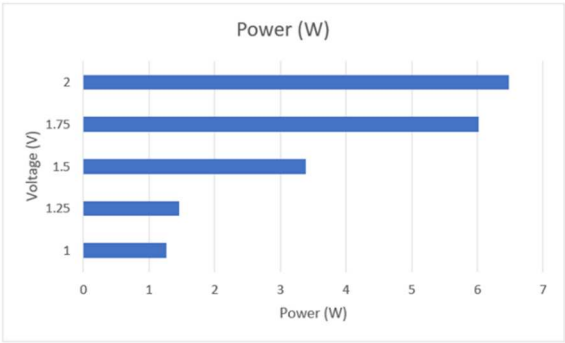

Figure 6. Power consumption of AR on Virtex 5 FPGA

V. Observation And Discussion

From the results it is observed that for both FPGA devices the power utilization rises as the voltage value rises. For low voltage, the power utilization is less. The power

utilization is increased for Virtex 5 FPGA as compared to Virtex 4 device which is described in fig 7. Therefore, it is observed that AR will consume low power for Virtex 4 device than Virtex 5 device.

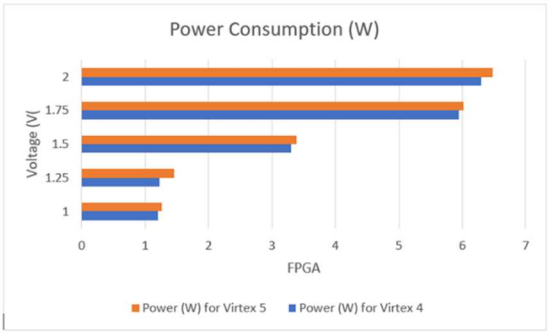

Figure 7. Power comparison for Virtex 5 and Virtex 4 FPGA

VI. Conclusion And Future Scope

In this paper, we build an address register (AR) that responds to voltage increases. The Xilinx 14.1 ISE tool was used to study the power fluctuation of an address register, and the address register code was created in the Verilog hardware description language. To evaluate the power consumption of AR, we used two FPGAs, one Virtex 4 and one Virtex 5. By raising the voltage from 1.0 V to 2.0 V, we were able to determine the change in on-chip power required by AR. We noticed that reducing the voltage lowers power consumption. At 2.0 V, power consumption is higher for both FPGAs. Therefore, to initiate the idea of Green Communication (GC) AR should be best suited with Virtex 4 FPGA. This paper discusses how to interface an address register with a Virtex 4 or a Virtex 5 FPGA. However, we may also connect the AR with other FPGAs such as the Cyclone, Artix-7, and Kintex-7, among others, to analyse power. We can also measure the frequency value, current value, and I/O standards to see how the power utilization varies, which will be useful in GC.

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